

Compact data acquisition and power supply system designed for hostile environment condition concerning radiation and magnetic field

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Abstract

A compact data acquisition and power supply system housed in a water cooled special crate has been designed for the readout of the TOF (Time Of Flight) detector of the Alice experiment at CERN.

The Crate called Alice-TOF-box contains a 12 slot VME64X bus that houses 2400 multi-hit 25ps TDC channels (TDC Readout Module: TRM), a local Trigger Module (LTM), a Clock Distribution Module (CPDM) and a Data Readout Module (DRM board) with two optical links and Ethernet.

The same crate hosts branch controlled power supply modules for the VME boards and the TOF detector front-end modules. The whole system shall be used close to the TOF detector and will work under moderate radiation and intense magnetic field (1.2 Gy/10 years TID, 5 KGauss).

The TDC boards house TDC chips developed by CERN/ECP-MIC Division (HPTDC). Due to the radioactive environment, an accurate choice of components is required and the VME boards implement protections from Single Event Latch-up (SEL) and from Single Event Upset (SEU).

I. INTRODUCTION

The ALICE (A Large Ion Collider Experiment) experiment will explore very high energy Ion-Ion interactions; the ALICE structure and detector are under construction at CERN's Large Hadron Collider (LHC).

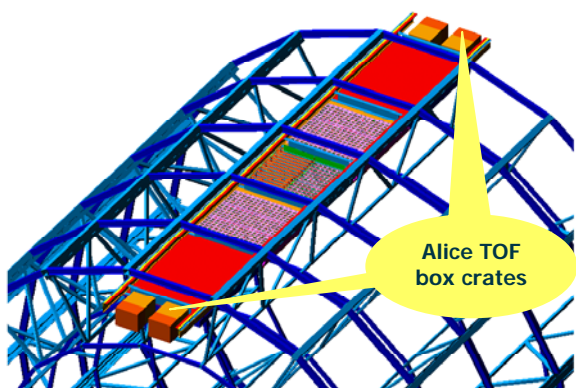


Figure 1: Alice TOF sector and the four crates at the ends.

Charged particles are identified in ALICE by the sub-detector Time-Of-Flight (TOF) [1]; TOF is a large area detector (150 m²) devoted to charged particle identification

made by Multigap Resistive Plate Chambers (MRPC). It's composed of 1638 MRPC strips with 157.248 readout pads, covering a cylindrical grid.

The TOF detector has to provide particle identification through precise time measurements of pulses induced by particles crossing the MRPCs (<100 ps time resolution). The readout system will be integrated into the detector and will feature mechanical and technical specifications suited to the TOF in order to guarantee the excellent resolution achieved by the test prototypes.

The readout system includes a series of VME 9U crates (with custom dimensions and features) which follow the "Front End Electronics" and host the TDC Readout Modules (TRM); such crates will be placed as close as possible to the detector, in an area not accessible during data acquisition.

In detail, the ALICE TOF will be made up by 18 Super Modules, like the one reported in Figure 1, each equipped with two readout crates on its sides. All the readout system must operate under huge magnetic field (up to 5000 Gauss) and moderate radiation; for this reason fans are not used and the device features a water cooling system with temperature sensors distributed on the boards.

A. Crate Description

The Alice-TOF-box prototype is shown in the following figure.



Figure 2: Alice-TOF-box prototype.

Each crate, based on a 12 slot VME64X Backplane, will host nine or ten 160x400mm TDC Readout Modules (TRM), thus achieving up to 2400 TDC channels per crate. The crate houses also the Data Readout Module (DRM), the Local

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Trigger Module (LTM) and the Clock Distribution Module (CPDM).

The VME boards and TOF detector Front End Electronics are supplied by branch controlled Low Voltage power supply modules contained in the Alice-TOF-box, namely two 3.3V/100A channels, eleven 2.7V/7A channels, one 5V/2A channel.

The block diagram in Figure 3 describes the crate architecture, the remote control of the power supplies and the box connections with the following ALICE/LHC sections: DAQ, Detector Control System (DCS), TOF Clock Distributor, LHC Trigger Control and TOF front end cards (FEA, FEAC).

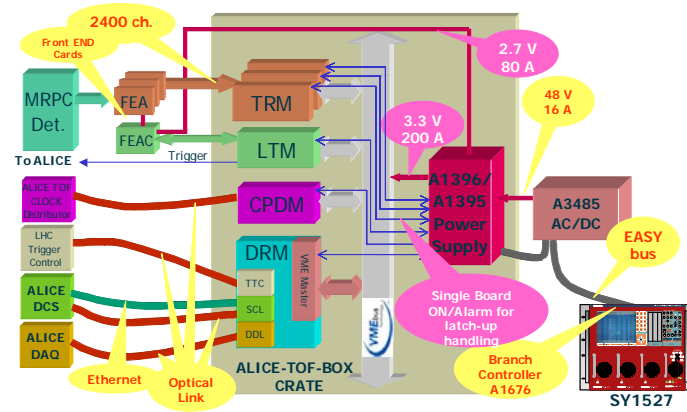


Figure 3: Alice TOF crate block diagram.

B. The TDC Readout Module (TRM)

The TRM board (Figure 4) is based on High Performance TDC (HPTDC) ASIC [2] developed by CERN/ECP-MIC Division. The CERN/ECP-MIC HPTDC is a General Purpose time-to-digital converter with multi-hit and multi event capabilities, its channels can be cascaded in order to obtain 8 channels with 25ps resolution.



Figure 4: TRM board.

Each TRM board features a VME 64X interface and houses 30 HPDTC and 10 temperature sensors on 10 piggy back boards, thus providing 240 25 ps TDC channels.

The TRM central FPGA acts as VME interface, readout controller and event manager; the readout controller section compensates on line the HPTDC Integral non linearity accessing a look-up table in a SRAM and provides calculation of hit length and subsequent data packing.

C. The Data Readout Module (DRM)

The DRM board (block diagram shown in Figure 5) provides the VME Master duties in the crate (data readout from TRM boards) and performs other functions, such as data transmission and communication with the DAQ system of ALICE experiment through Data Detector Link (DDL) [3], reception and computing of trigger signals through Timing Trigger Control receiver (TTCrx) [4], VME bus access through a slow control optical link (Slow Control Link: SCL) and remote programming of FPGA on VME boards in the crate.

The DRM performs also L2 event building and data sniffing from DDL link providing useful online information for detector debug and data quality monitor.

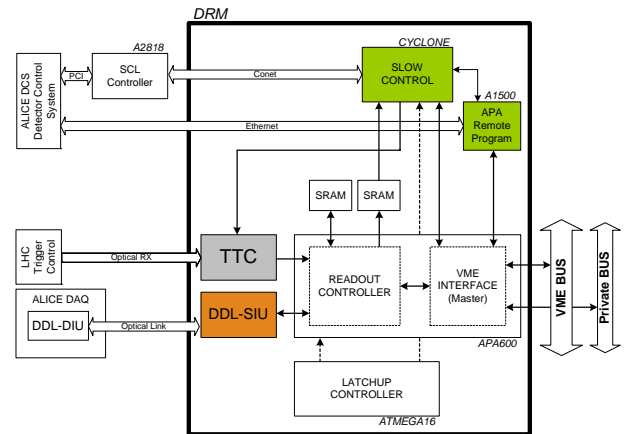


Figure 5: DRM board.

The DRM Slow Control section houses one Linux embedded Single Board Computer [5] (Mod. A1500 with 200MIPS RISC). The DRM Slow Control section can be accessed via Optical Fiber (1.25 GHz Optical link), via Ethernet 10/100 Mbit/sec and via the DDL interface.

TTC section houses the TTCrx (Timing, Trigger and Control Receiver ASIC for LHC Detectors). The TTCrx acts as an interface between the Timing Trigger and Control distribution (TTC) system for LHC detectors and its receiving end users. The ASIC delivers the clock together with control and synchronisation information to the front-end electronics controllers in the detector.

The DDL-SIU section houses, on a piggy back board, the Source Interface Unit developed by the ALICE collaboration in the Detector Data Link framework. The ALICE Detector Data Link (DDL) [3] is a high-speed optical link designed to

interface the readout electronics of ALICE detectors to the DAQ computers.

D. The Local Trigger Module (LTM)

The LTM provides the signal set up for trigger, for the slow control of some detector parameters (low voltages, temperature) and for the production of the threshold voltages of the Front End Cards (FEA). Moreover each LTM provides the logical trigger logic of the FEAC signals which is then sent to the ALICE trigger section.

E. The Clock Distribution Module (CPDM)

The CPDM board is hosted only in one crate every two. It receives through the unimode optical link the LHC clock signal, translates it into a LVDS level and distributes it to the TRMs, thus providing the 24x fan out function with jitter <10 ps. Moreover the CPDM provides the 12x fan out of the strobe pulse from the DRM, towards the pads. The CPDM is not handled via VME bus.

F. Power Supply Architecture

The power supply section is developed from the EASY (Embedded Assembly SYstem) modules [6] and is composed by one Mod. A1396 and two Mod. A1395, branch controlled power supply modules, whose position in the crate is described in Figure 6. The Mod. A1396 houses a General COntroller device (GECO) and the front end power supply.

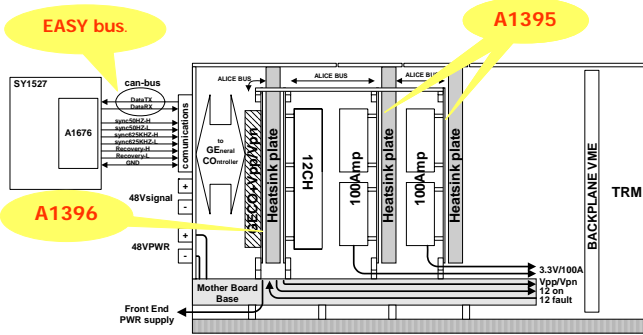


Figure 6: Power Supply Block diagram.

The Mod. A1396 is connected to a branch controller board (A1676A) housed in a CAEN SY1527 System [7], located in the experimental hall, where the magnetic field is about 60 Gauss. four SY1527 placed around the detector house two branch controllers A1676A each, connected to 18 crates (one TOF quadrant) via EASY bus (Figure 7). The whole system is supplied by 12 customized 48 V AC/DC converters (Mod. A3485), designed to work in a moderately hostile area and controlled as low voltage channels through a GECO device.

The Mod. A1396 provides eleven 2.7V/7A channels and one 5V/2A channel and has two temperature sensors; the Mod. A1395 provides one 3.3V/100A channel and has four temperature sensors.

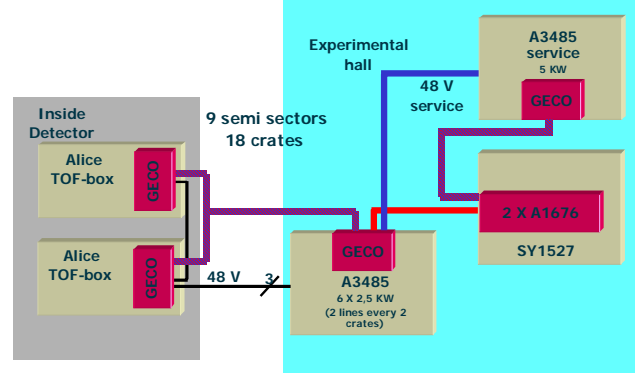


Figure 7: Logical scheme of LV power supply for a TOF quadrant.

II. HOSTILE ENVIRONMENT

The crate is designed to work in a slightly hostile environment, with moderate radiation and intense magnetic field. Architecture and components will then guarantee resistance under radiation and magnetic fields; fan cooling is replaced by water cooling.

A. Radiation Tolerance

The crate will operate in a moderate hostile environment for what concerns total levels of radiation (Table 1) [8]. If damages for total integrated dose are likely to be negligible, protections for latchups are needed, as well as an adequate SEU protection/detection.

Table 1: The expected doses and hadron fluences for 10 years

Total dose	1.2 Gy
Neutron fluence (>20 MeV):	$2.1 \cdot 10^9 \text{ cm}^{-2}$
Max Charged hadron/neutron (>20MeV) fluence rate	89 Hz/cm ²

The SEL protection is achieved by dividing each board in sections with separate power supply. Each section is independently monitored and "protected" by a current-limiting device (MAX893L), while an Atmel μC handles the section ON/OFF status: if SEL faults are signalled by the relevant indicators, the Atmel μC detects them and switches off the sections with SEL faults in order to correct the SEL condition and to avoid permanent damages.

The SEU protection/detection architecture is based on radiation tests carried on the key components of the ALICE TOF readout modules [9]. Such tests reported an esteem of the SEU rates and helped to select the proposed components. The implemented solution was then the following: Flash based FPGA Actel ProAsic Plus (APA 750), which are substantially immune to SEU in the configuration bits, are used for vital sections, while other sections use RAM based ALTERA FPGA (reprogrammed after a CRC error). The SRAM implements a CRC check in order to identify NOT valid data. No SEE effect was observed in the Flash and in the Atmel μC (ATMEGA). The HPTDC look-up tables will be periodically monitored via CRC and require reload from Flash memory.

B. Cooling System

The presence of a huge magnetic field does not allow to use fans in order to cool down the whole crate. Heat dissipation of crates and boards takes place thanks to water coolers, placed on both the crate's sides. The Cooling System is compliant to the following requirements: the electronics maximum temperature is 100°C, the inlet cooling water temperatures (T_{in}) is 15°C and max temperature raise of the cooling water (T_{raise}) is 7 °C, the available flow for each crate is 4 l/min. The total power dissipated by an Alice-TOF-box is 1 kWatt (450 W for 10 TRM board).

C. Cooling System Layout

The following figures shows the Layout system of the TRM boards which is assembled with "card-lok" and aluminium heatsink plates.

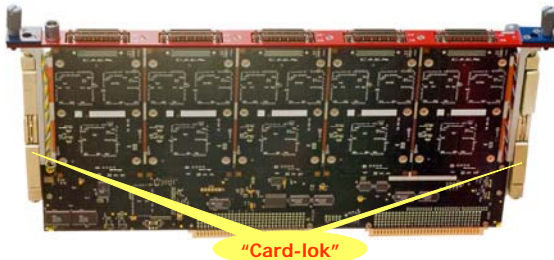


Figure 8: TRM Card lok.

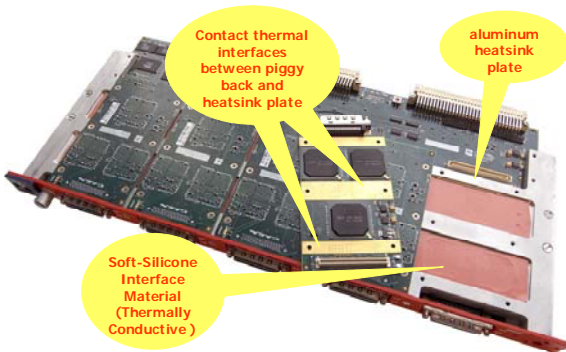


Figure 9: TRM heatsink plate.

The following figure shows the cooling channel integrate on the crate, i.e. the heatsink plate/"card-lok" connection with the crate heat exchangers.

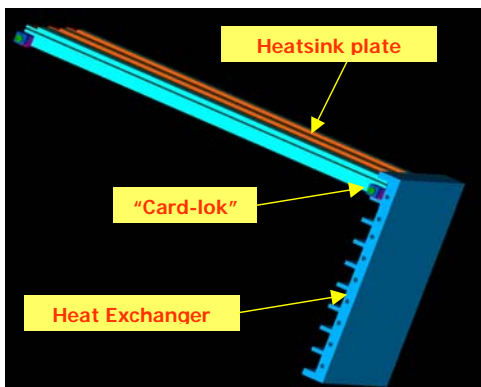


Figure 10: Cooling System Layout.

III. PROTOTYPE TEST

The Alice-TOF-box prototype was tested in the first place in CAEN in order to analyse the cooling system; Figure 11: shows the temperature traces of the TRM boards sensors; it can be noticed that the temperature ranges between 30 and 40°C, thus remaining within the requirements limits. The temperature peak in Figure 11 corresponds to an off/on cycle of the cooling liquid flow.

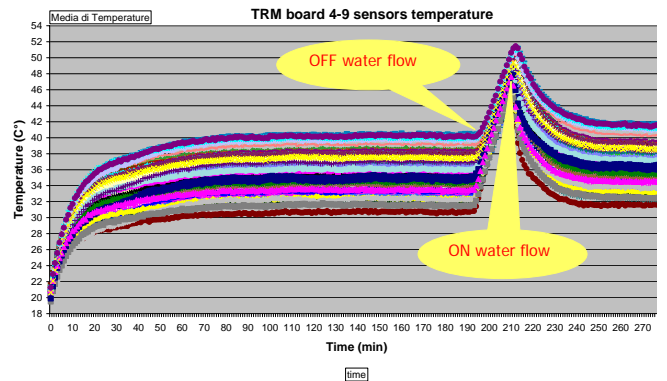


Figure 11: Cooling System Test (no magnetic field) room temperature: 27° C.

Prototype tests for Power supply and Cooling system have been performed in the final position, during the ALICE solenoid and dipole magnetic field mapping [10]. No loss in communication and power quality was observed, with a magnetic field value of 6750 gauss, oriented like the one foreseen inside the ALICE experiment

Figure 12 shows a thermal image of the Alice TOF-Box prototype front panel, after about 4 hours of prototype test (5300 Gauss Magnetic Field); it can be noticed that the maximum detected surface temperature is 25°C: this means that the cooling system works properly even in a magnetic field.

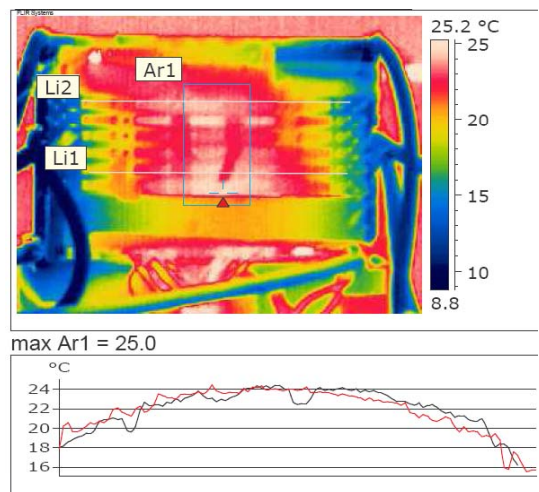


Figure 12: Thermal image after 4 hours of prototype test (magnetic field: 5300 Gauss, room temperature: 21° C)

IV. CONCLUSIONS

The experience on the development of the integrated power supply and data acquisition system described in this article, gives CAEN today the know-how to produce “hostile area” tolerant VME bus crates and to support physicists in the development of VME boards suitable to near-Detector operation.

V. ACKNOWLEDGMENTS

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VI. REFERENCES

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